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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/606,159	06/29/00	NAGAI T	037267/0135

EXAMINER	
BROCK II, P	
ART UNIT	PAPER NUMBER
2815	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No.	Applicant(s)	
	09/606,159	NAGAI ET AL.	
	Examin r	Art Unit	
	Paul E Brock II	2815	

-- The MAILING DATE of this communication appears on the cover she t with the correspond nce address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 April 2001* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *21-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *21-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. *09/124,851* .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

15) ☐ Notice of References Cited (PTO-892)
16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
17) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
18) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
19) ☐ Notice of Informal Patent Application (PTO-152)
20) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 21 and 24 are rejected under 35 U.S.C. 112, second paragraph, as failing to set forth the subject matter which applicant(s) regard as their invention. Evidence that claim 21 fail(s) to correspond in scope with that which applicant(s) regard as the invention can be found in Paper No. 1 filed 6-29-00. In that paper, applicant has stated on page 12, lines 22 – 23 that the control gate (7) doubles as a word line, and this statement indicates that the invention is different from what is defined in the claim(s) because step (a) refers to "forming a plurality of field insulating films in parallel with one another and perpendicular to a plurality of word lines on a semiconductor substrate;" however, steps (d) and (e) refer directly to the process of making a control gate. It is not clear how, if the control gate and the word lines are the same thing as was originally disclosed, the plurality of field insulating films can be parallel to something at the time of its formation has not yet been formed.

3. Claims 21 and 24 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. It is not clear how in step (c) "forming a plurality of first polysilicon layers in parallel with one another perpendicularly to said plurality of word lines;" it is possible to form layers of polysilicon perpendicular or parallel to anything. For example, "forming ... polysilicon layers" would be interpreted by one of ordinary skill in the art to be a blanket layer of

polysilicon over a surface of the existing semiconductor substrate. It is not clear how a blanket layer of anything can be perpendicular to a line formed on a substrate.

4. Claim 21 recites the limitations "said top portion of the plurality of bit studs" and "said bottom portion of the plurality of bit studs" in the last line of the claim. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

5. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

6. Claims 21, 22 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kamiya et al. in view of Kim.

Kamiya et al. discloses a method of fabricating an EEPROM semiconductor device in figures 1 – 7.

With regard to claim 21, Kamiya et al. discloses in figures 1 and 4 forming a plurality of field insulating films (101) in parallel with one another on a semiconductor substrate (100). Kamiya et al. discloses in figure 1 forming a first gate insulating film (103 and 106a) in each of active regions. Kamiya et al. then discloses in figure 1 forming a plurality of first polysilicon layers (107a) in parallel with one another. Kamiya et al. further discloses in figure 1 forming a second gate insulating film (106) and a second polysilicon layer (107) all over the product resulting from the above steps. Kamiya et al. then discloses in figure 1 patterning the second polysilicon layer, the second gate insulating film, and the first polysilicon layer to thereby form a control gate (107) and a floating gate (107a). Kamiya et al. also discloses in figure 1 forming

drain (109a) and source (109) regions. Kamiya et al. also discloses in figure 1 forming a first interlayer insulating layer (111) over the product resulting from the above steps. Kamiya et al. discloses in figure 4 forming a first metal wiring layer which is patterned so as to form both a common source line (114 and 115) extending in parallel with one another and connecting source regions to one another and a plurality of bit studs (113 and 115) extending to the drain regions. Kamiya et al. discloses in figures 6 and 7 forming a second metal wiring layer (118a) which is patterned so as to form a bit line and connecting the drain regions with each another. Kamiya et al. does not disclose forming a second interlayer insulating layer all over the product resulting from the steps before forming the second metal wiring layer, nor does Kamiya et al. disclose the bit line having a top portion and a bottom portion. Kim teaches in figure 6 and column 3, lines 10 – 15 forming an interlayer insulating layer all over a product before forming a second metal wiring layer. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the interlayer insulating film of Kim in the process of forming a second metal wiring layer of Kamiya et al. in order to form a bit line as stated by Kim in column 3, lines 10 – 15. Kim also discloses in figure 10c a bit line (80) having a top portion and a bottom portion with the top portion being wider than the bottom portion. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the bit line with a top and bottom portion of Kim in the method of Kamiya et al. in order to form a bit line in a long rod shape in the direction of the Y-axis and is shared by cell transistor's drains adjacent in the direction of the Y-axis as stated by Kim in column 11, lines 23 – 25. It is further obvious that in the method of Kamiya et al. and Kim the bottom portion of the bit line is connected to the top

portion of the plurality of bit studs and the bottom portion of the plurality of bit studs is connected to the drain regions.

With regard to claim 22, Kamiya et al. discloses in column 4, lines 46 – 51 that the second gate insulating film has a three-layer structure of oxide/nitride/oxide films.

With regard to claim 24, Kamiya et al. discloses in figures 1 and 4 forming a plurality of field insulating films (101) in parallel with one another on a semiconductor substrate (100). Kamiya et al. discloses in figure 1 forming a first gate insulating film (103 and 106a) in each of active regions. Kamiya et al. then discloses in figure 1 forming a plurality of first polysilicon layers (107a) in parallel with one another. Kamiya et al. further discloses in figure 1 that forming a second gate insulating film (106) and a second polysilicon layer (107) all over the product resulting from the above steps. Kamiya et al. then discloses in figure 1 patterning the second polysilicon layer, the second gate insulating film, and the first polysilicon layer to thereby form a control gate (107) and a floating gate (107a). Kamiya et al. also discloses in figure 1 forming drain (109a) and source (109) regions. Kamiya et al. also discloses in figure 1 forming a first interlayer insulating layer (111) over the product resulting from the above steps. Kamiya et al. discloses in figure 4 forming a first metal wiring layer which is patterned so as to form both a common bit line (114 and 115) extending in parallel with one another and connecting bit regions to one another and a plurality of source studs (113 and 115) extending to the source regions, the plurality of source studs of Kamiya have a top portion (connected to the source line) and a bottom portion (connected to the source region) with the top portion of the plurality of source studs being wider than the bottom portion of the plurality of source studs. Kamiya et al. does not disclose forming a second metal wiring layer which is patterned so as to form a common source

line connecting the drain regions to one another. Kamiya et al. does not disclose forming a second interlayer insulating layer all over the product resulting from the steps before forming the second metal wiring layer. Kim teaches in figure 8g and column 6, lines 51 – 55 forming a first metal wiring layer which is patterned so as to form both a bit line 71 extending almost in parallel with field insulating films and connecting drain regions to one another, and an extended common source line (73) connecting the source region to a later mentioned common source line. While Kim describes the feature 71 as a source line, it is accepted in the art that a process used to make features of a source line can be interchanged with a process used to make a drain line as long as the opposite is true. Kim teaches in figure 6 and column 3, lines 10 – 15 forming an interlayer insulating layer all over a product. Kim teaches in figure 8g forming a second metal wiring layer (80) which is patterned so as to form a common source line connecting the source regions with each another, the common source line having a top portion and a bottom portion with the top portion of the common source line being wider than the bottom portion of the common source line, wherein the bottom portion of the common source line is connected to a top portion (73) of a plurality of source studs and a bottom portion of the plurality of source studs (69) is connected to a source region. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the wiring processes and interlayer insulating film of Kim in the fabrication of an EEPROM semiconductor device of Kamiya et al. in order to overcome the integration limitations caused by standard photolithography methods as stated by Kim in column 1, lines 52 – 60.

7. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kamiya et al. in view of Kim. as applied to claim 21 above, and further in view of Yonemoto.

Kamiya et al. does disclose in column 5, lines 62 – 63 that the second wiring layers are composed of aluminum. Kamiya et al. does not disclose forming the first wiring layer of aluminum. Yonemoto does disclose forming a first wiring layer composed of aluminum in column 5, lines 8 – 11. It would have been obvious to use the aluminum wiring of Yonemoto in the process of Kamiya et al. in view of Kim in order to form signal lines to connect to the source region as stated by Yonemoto in column 5, lines 8 – 11.

8. Claims 25 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kamiya et al. in view of Kim. as applied to claim 24 above, and further in view of Cacharelis et al. Kamiya et al. does not disclose forming backing wiring layers. Cacharelis et al. teaches in figure 20a forming backing wiring layers (490 and 500) connecting to a control gate at a certain interval and are constituted of a second metal wiring layer. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the backing wires of Cacharelis et al. in the method of Kamiya et al. in view of Kim in order to form a word lines as stated in column 5, lines 50 – 53.

9. Applicant's arguments filed April 9, 2001 have been fully considered but they are not persuasive. While Kamiya et al. does not disclose a bit line that comprises two portions, Kim does disclose a bit line comprising two portions as described above. The examiner fails to find a difference in the bit line of Kim and that of the claimed invention. Further, the applicant argues

that the bit studs of Kim do not comprise a top portion and a bottom portion. As can be seen above, Kim does have bit studs that comprise a top portion (73) and a bottom portion (69), the bottom portion being connected directly to the drain regions. The examiner fails to find a difference in the studs of Kim and that of the claimed invention.

Conclusion

10. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul E Brock II whose telephone number is (703)308-6236. The examiner can normally be reached on 8:30 AM-5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (703)308-1690. The fax phone numbers for the

organization where this application or proceeding is assigned are (703)308-7722 for regular communications and (703)308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

Paul E Brock II
May 9, 2001

EDDIE LEE
SUPERVISORY PATENT EXAMINER
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